• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. It combines one N channel MOSFET and one P channel MOSFET

• Features

■AEC-Q101 Qualified

■Low $R_{DS(ON)}$ to minimize conductive loss

■Dual DIE in one package

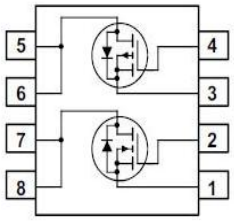
■Low Thermal resistance

•Application

■BLDC Motor driver

■Load switch

• Product Summary



V_{DS1}= 60V

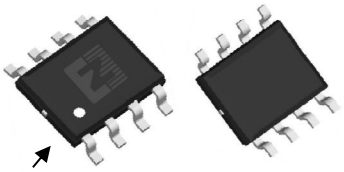
V_{DS2}= -60V

$R_{DS(ON)1}$ = 43mΩ

$R_{DS(ON)2}$ = 57mΩ

I_{D1}= 4.5A

I_{D2}= -4A



pin1

SOP-8

•Ordering Information:

Part NO.	ZMCA88601S
Marking	ZMC88601
Packing Information	REEL TAPE
Basic ordering unit (pcs)	4000

•N Channel Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage①	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	4.5	A
	I_D	T_C=75℃	4	A
	I_D	T_C=100℃	3	A
Pulsed Drain Current	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	13.5	A
Total Power Dissipation	P_D	T_C=25℃	4	W
Total Power Dissipation	P_D	T_A=25℃	0.7	W
Operating Junction Temperature	T_J		-55 to +150	℃
Storage Temperature	T_{STG}		-55 to +150	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=10V, Rg=25Ω,	10	mJ
		L=0.5mH, V_{GS}=10V, Rg=25Ω,	21	mJ
ESD Level (HBM)	CLASS 1C			

●P Channel Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		-60	V
Gate-Source Voltage②	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	-4	A
	I_D	T_C=75℃	-4	A
	I_D	T_C=100℃	-3	A
Pulsed Drain Current	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	-12	A
Total Power Dissipation	P_D	T_C=25℃	4	W
Total Power Dissipation	P_D	T_A=25℃	0.7	W
Operating Junction Temperature	T_J		-55 to +150	℃
Storage Temperature	T_{STG}		-55 to +150	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=-10V, Rg=25Ω,	30	mJ
		L=0.5mH, V_{GS}=-10V, Rg=25Ω,	54	mJ
ESD Level (HBM)	CLASS 2			

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	34	°C/W
Thermal resistance, junction-ambient③	R_{thJA}		-	180	°C/W
Soldering temperature	Tsold		-	260	°C

•N Channel Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	1.2	1.7	2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= 60V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D= 4.5A		43	50	mΩ
		V_{GS}=4.5V, I_D= 4A		75	85	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5V, I_{SD} = 2A		10		s
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = 4.5A			1.3	V

•N Channel Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=25V	-	823	-	pF
Output capacitance	Coss		-	33	-	
Reverse transfer capacitance	Crss		-	19	-	
Gate Risistance	Rg	f = 1MHz	-	1		Ω
Total gate charge	Qg	V_{DD} =25V, I_D =3A, V_{GS} =10V	-	12	-	nC
	Qg (4.5v)		-	5	-	
Gate - Source charge	Qgs		-	1.6	-	
Gate - Drain charge	Qgd		-	2.6	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V, R_G =3.3Ω, I_D =20A	-	2	-	ns
Turn-ON Rise time	t_r		-	3	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	10	-	ns
Turn-Off Fall time	t_f		-	7.5	-	ns

●P Channel Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =-250uA	-60			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =-250uA	-1.2	-1.7	-2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= -60V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=-10V, $I_{D=}$ -4A		57	74	mΩ
		V_{GS}=-4.5V, I_D= -3A		76	100	mΩ
Forward Transconductance	g_{FS}	V_{DS} =-5V, I_{SD} = -2A		9		s
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = -4A			1.3	V

●P Channel Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=-25V	-	1380	-	pF
Output capacitance	Coss		-	101	-	
Reverse transfer capacitance	Crss		-	67	-	
Gate Risistance	Rg	f = 1MHz	-	8		Ω
Total gate charge	Qg	V_{DD} = -25V, I_D = -3A, V_{GS} = -10V	-	21	-	nC
	Qg (-4.5v)		-	9	-	
Gate - Source charge	Qgs		-	3.5	-	
Gate - Drain charge	Qgd		-	3.6	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=-10V,V_{DS}=-15V, R_G =3.3, I_D =-10A	-	20	-	ns
Turn-ON Rise time	t_r		-	174	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	43	-	ns
Turn-Off Fall time	t_f		-	10.4	-	ns

• N Channel characteristics curve

Fig.1 Gate-Charge Characteristics

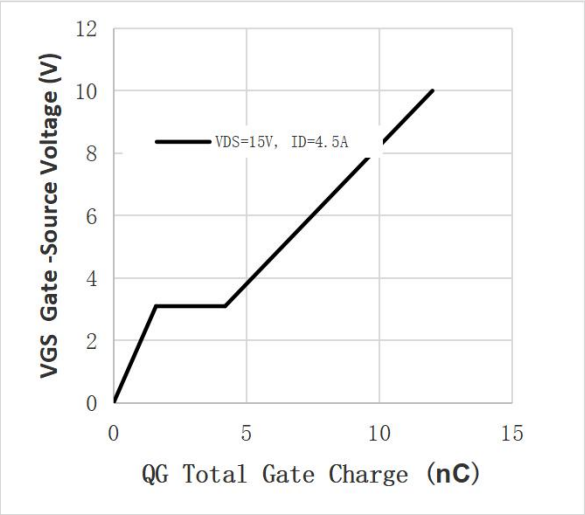


Fig.2 Capacitance Characteristics

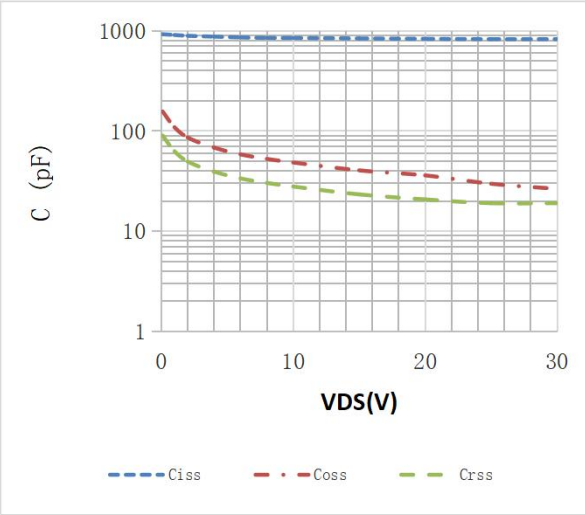


Fig.3 Power Dissipation

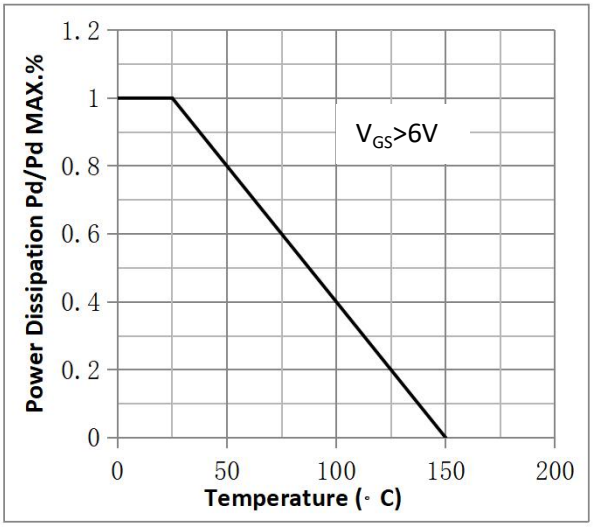


Fig.4 Typical output Characteristics

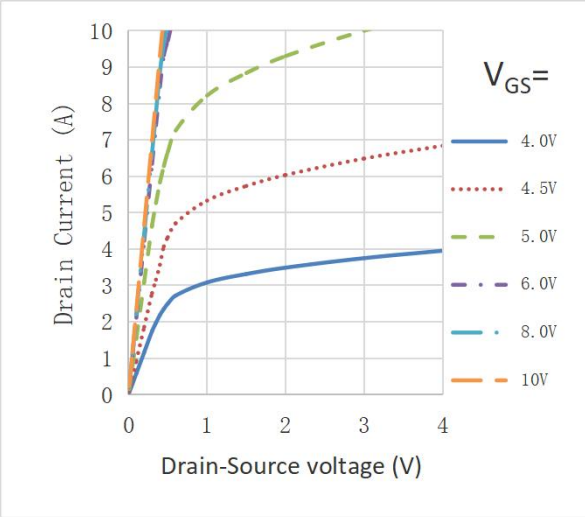


Fig.5 Threshold Voltage V.S Junction Temperature

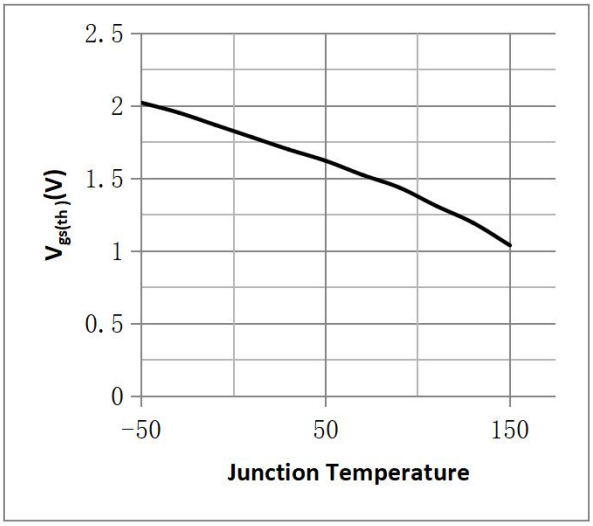


Fig.6 Resistance V.S Drain Current

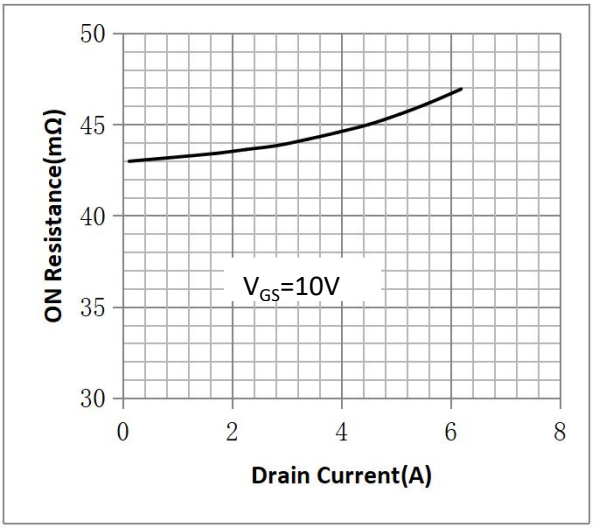


Fig.7 On-Resistance VS Gate Source Voltage

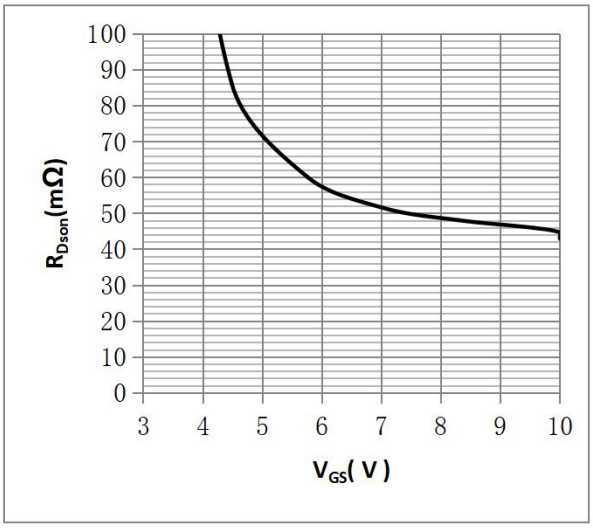


Fig.8 On-Resistance V.S Junction Temperature

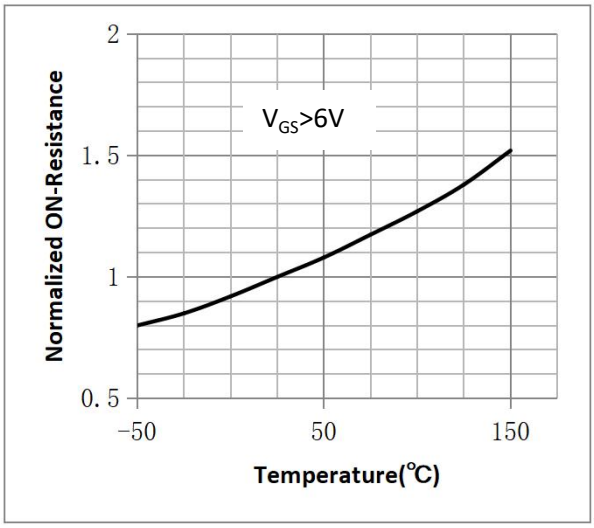


Figure 9. Diode Forward Voltage vs. Current

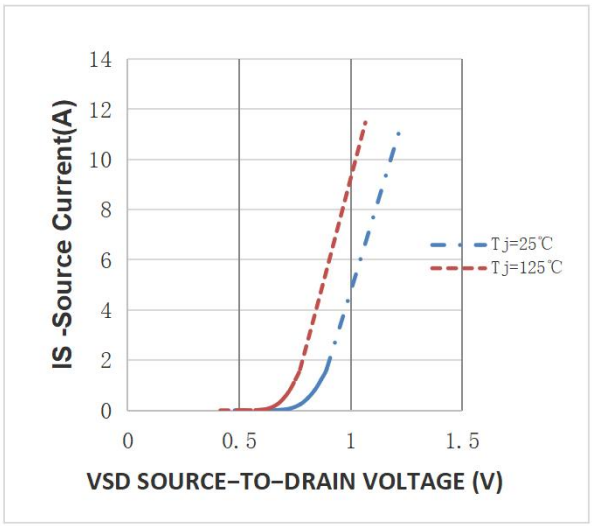


Figure 10. Transfer Characteristics

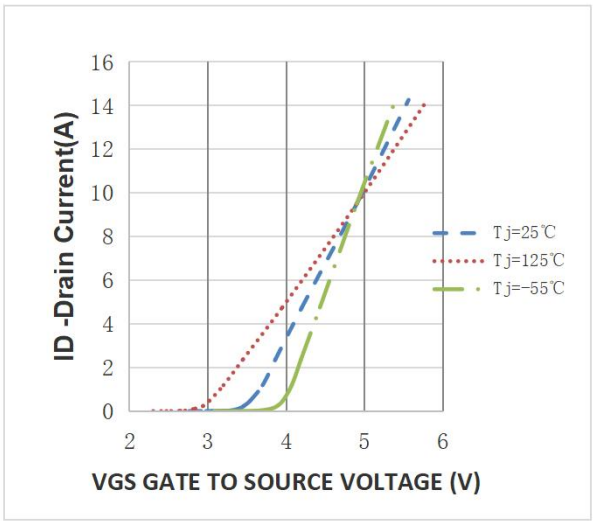


Fig.11 Safe Operating Area

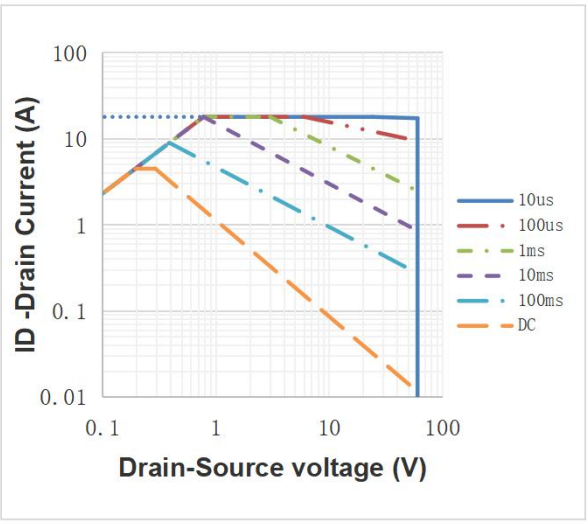
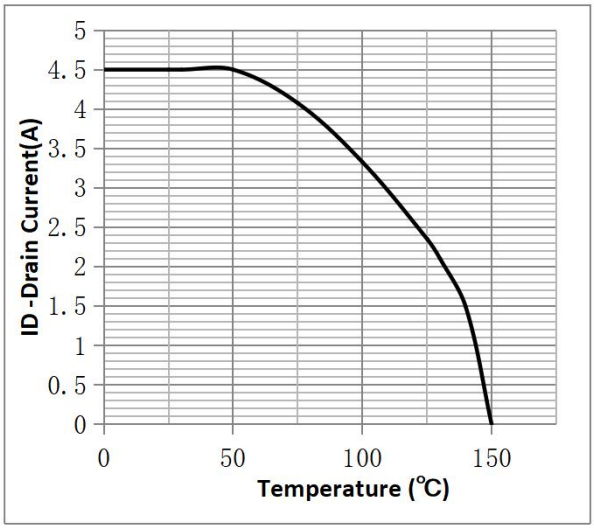


Fig.12 ID vs. Case Temperature④



•p Channel characteristics curve

Fig.1 Gate-Charge Characteristics

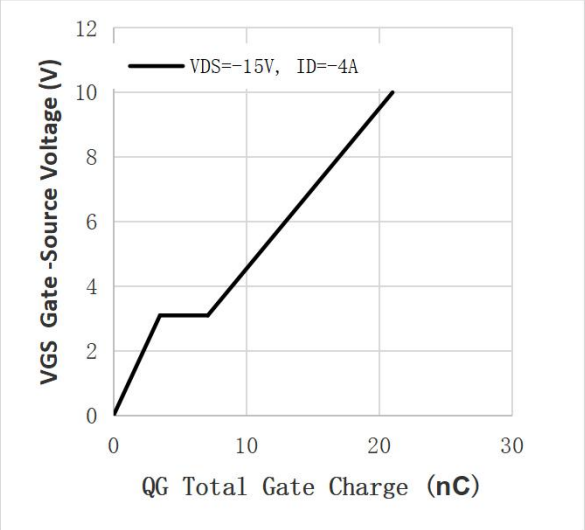


Fig.2 Capacitance Characteristics

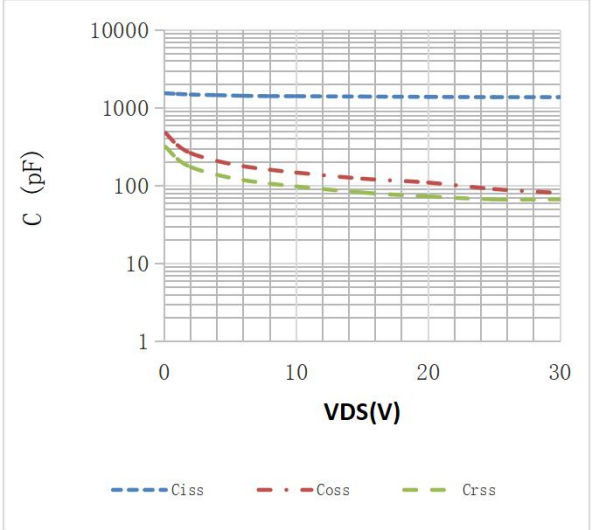


Fig.3 Power Dissipation

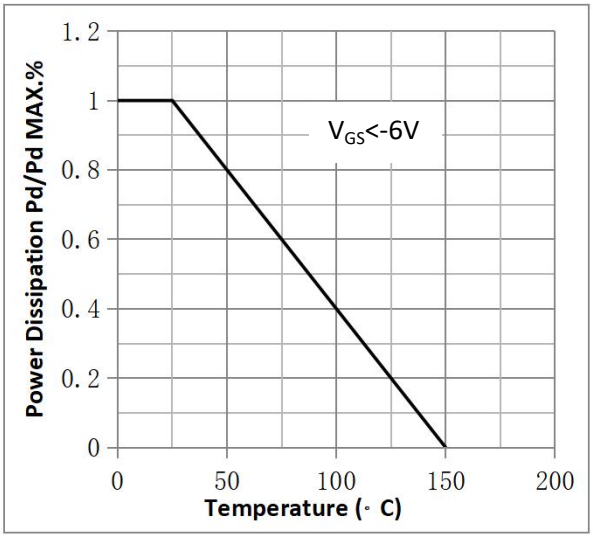


Fig.4 Typical output Characteristics

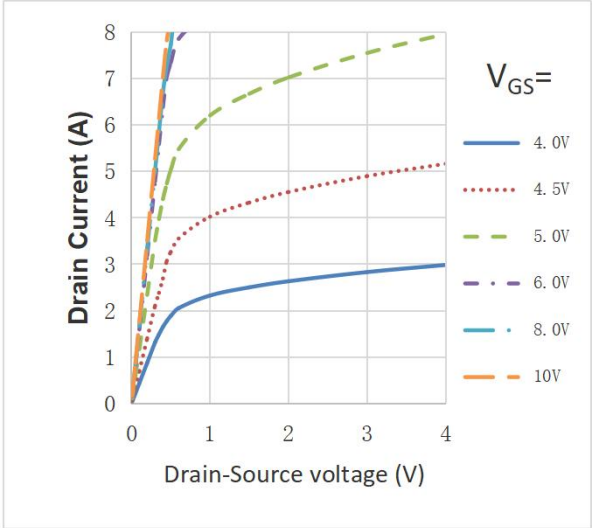


Fig.5 Threshold Voltage V.S Junction Temperature

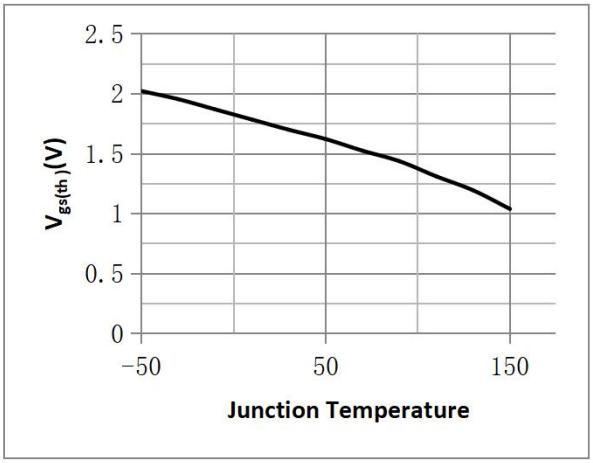


Fig.6 Resistance V.S Drain Current

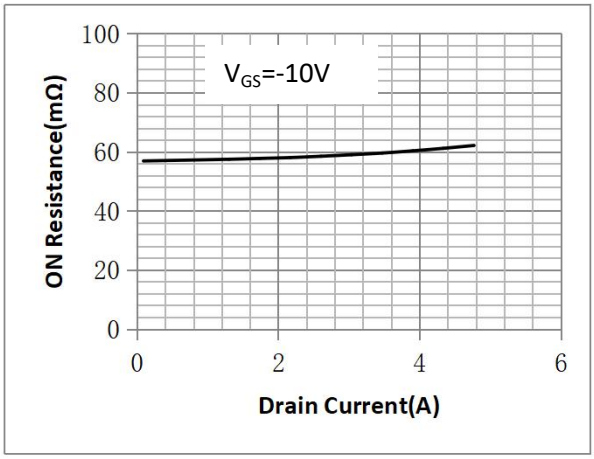


Fig.7 On-Resistance VS Gate Source Voltage

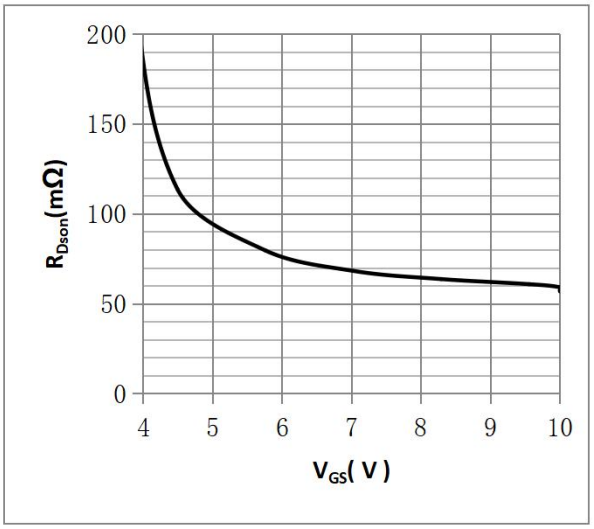


Fig.8 On-Resistance V.S Junction Temperature

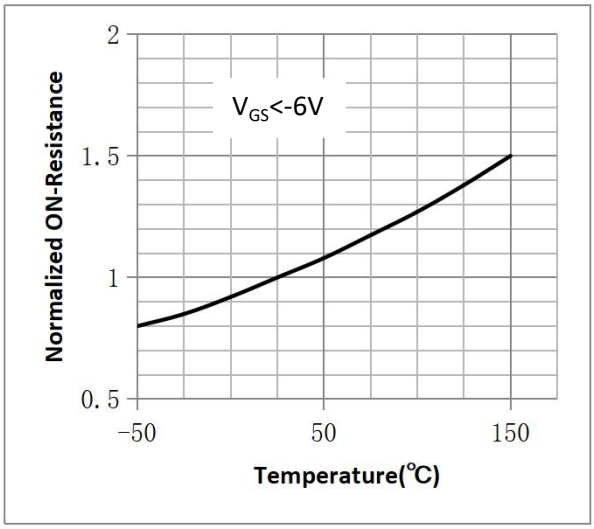


Figure 9. Diode Forward Voltage vs. Current

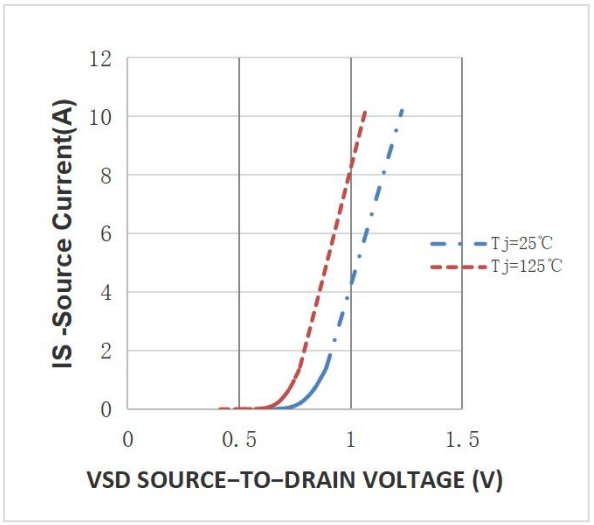


Figure 10. Transfer Characteristics

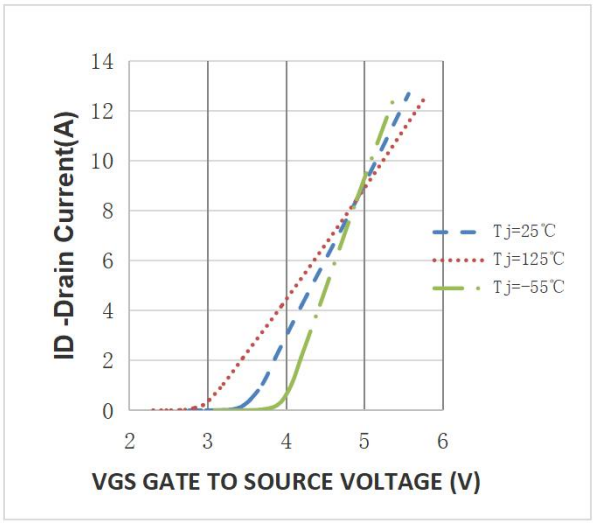


Fig.11 Safe Operating Area

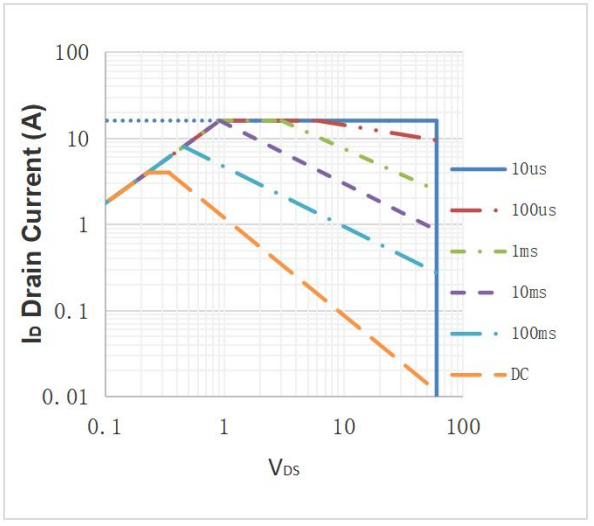
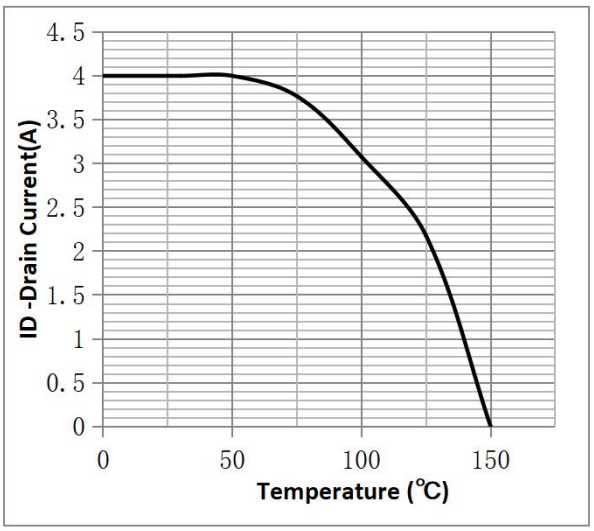
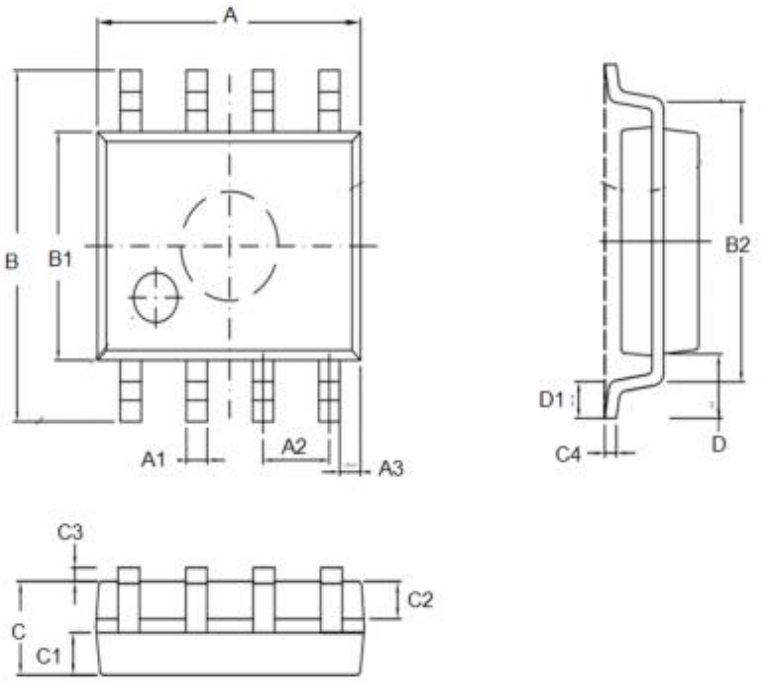


Fig.12 ID vs. Case Temperature④



●SOP-8 Package Outline



SYMBOL	min	TYP	max	SYMBOL	min		max
A	4.80		5.25	C	1.30		1.75
A1	0.37		0.49	C1	0.55		0.75
A2		1.27		C2	0.55		0.65
A3		0.41		C3	0.05		0.20
B	5.80		6.20	C4	0.10	0.20	0.23
B1	3.80		4.10	D		1.05	
B2		5.00		D1	0.40		0.62

Note:

① Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=+20V/-10V, Tj=175℃, t=1000 hours；

② Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=-20V/+10V, Tj=175℃, t=1000 hours；

③ Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

④ Practically the current will be limited by PCB, thermal design and operating temperature. VGS=10V (N channel)/-10V(P channel).

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Revision History

Version	Date	Change
A	2021.10.16	NEW
B	2021.10.13	Modifyied the ID curve
C	2023.11.1	Modifyied the ID curve